Technology Mapping of Reversible Circuits to Clifford+T Quantum Circuits

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***Abstract*—The Clifford+T quantum gate library has attracted much interest in the design of quantum circuits, particularly since the contained operations can be implemented in a fault-tolerant manner. Since fault tolerant implementations of the T gate have very high latency, synthesis and optimization are aiming at minimizing the number of T stages, referred to as the T-depth.**

In this paper, we present an approach to map mixed polarity multiple controlled Toffoli gates into Clifford+T quantum circuits. Our approach is based on the multiple control Toffoli mapping algorithms proposed by Barenco et al. , which are given T-depth optimized Clifford+T translations. Experiments show that our approach leads to a significant T-depth reduction of 54% on average.

I. Introduction

Quantum computing has shown promising results, e.g., for solving certain problems exponentially faster than any known classical algorithm by exploiting quantum mechanical effects. In contrast to Boolean logic, quantum bits (qubits) not only represent the classical 0 and 1 states but also any complex combination or *superposition* of both, leading to a significant speed-up in computing. The Deutsch-Jozsa algorithm [1] as well as Shor's factorization algorithm [2] are famous examples showing the power of quantum computing.

Since many underlying quantum algorithms include a Boolean component, the synthesis of such components is typically conducted by a two-stage procedure: (i) a reversible circuit realizing the Boolean component is generated for which existing synthesis algorithms such as [3] are used, (ii) mapping techniques are applied to transform the reversible circuit into a functionally equivalent quantum circuit [4]–[6]. The second stage is typically divided into further stages where a reversible circuit is first mapped into NOT, CNOT and Toffoli gates; those gates are then individually mapped to the relevant low-level library. While this layered approach allows convenient reuse of circuits between applications, the results are typically non-optimal as the structure of the high-level circuit may allow low-level gates to be omitted. As a result, researchers have proposed [6], [7] optimized mappings directly from reversible circuits into low-level or intermediate quantum gate libraries, e.g., the NCV [4] library or NCT+Peres. Such mappings avoid the overhead of applying primitive gate optimization and in some cases achieve better results due to human insight.

Recently, there has been particular interest in quantum circuits composed of Clifford+T gates where a major objective is to minimize the number of T gates and particularly the T-depth of the circuit. This is motivated by the importance of fault tolerance in quantum computations [8] and by the fact that the cost of the fault tolerant implementation of a T gate can exceed the cost of implementing a Clifford gate by a factor of 100 or more [9]. While automated Clifford+T optimization techniques exist [10], no optimized mapping approaches have yet been developed for the Clifford+T library.

In this paper we present mapping schemes based on existing algorithms to produce circuits of low T-depth. No previous mapping scheme has considered this quantum cost metric explicitly. We present

1) an improved algorithm to map c-control MPMCT gates into Clifford+T circuits using $(c-2)$ helper lines, called ancillas, and
2) an improved algorithm to map c-control MPMCT gates into Clifford+T circuits using one ancilla

These algorithms are then used to map reversible circuits into Clifford+T quantum circuits, taking into account the ancillas available at each reversible gate.

This optimized reversible circuit mapping approach, integrated into our design flow for quantum circuits, allows for significant T-depth reduction compared to existing mapping approaches and Clifford+T circuit optimization algorithms. As confirmed by an experimental evaluation, improvements of the T-depth of up to 65% can be observed. This clearly demonstrates the efficiency of our approaches on optimizing the cost of Clifford+T quantum circuit.

II. Background

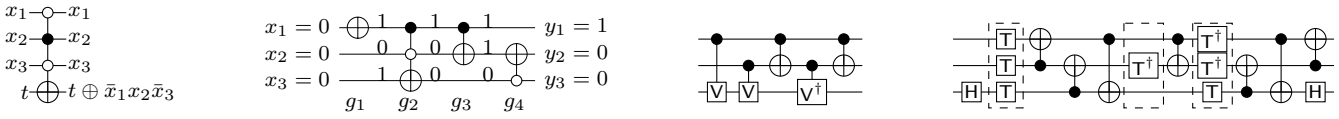
This section briefly introduces the basics on reversible and quantum circuits.

A. Reversible Circuits

Let $\mathbb{B} = \{0, 1\}$ denote the *Boolean values*. We refer to $\mathcal{B}_{n,m} = \{f \mid f\colon \mathbb{B}^n \to \mathbb{B}^m\}$ as the set of all *Boolean multiple-output functions* with n inputs and m outputs.

Definition 1 (Reversible function): A function $f \in \mathcal{B}_{n,m}$ is called *reversible* if f is bijective, i.e., if each input pattern is uniquely mapped to an output pattern, and vice versa. Otherwise, it is called *irreversible*.

Reversible functions on n bits are realized by circuits consisting of at least n lines over multiple controlled Toffoli gates [3].



(a) MPMCT gate (b) Reversible circuit (c) NCV circuit (d) Clifford+T circuit

Fig. 1: Reversible and quantum circuits

Definition 2 (Toffoli gate): Given a set of variables $X = \{x_1, \ldots, x_n\}$, a *mixed polarity multiple controlled Toffoli (MPMCT)* gate $\mathrm{T}(C, t)$ has *control lines* $C = \{x_{j_1}, x_{j_2}, \ldots, x_{j_c}\} \subset X$ and a *target line* $t \in X \setminus C$. The gate maps $t \mapsto t \oplus (x_{j_1}^{p_1} \wedge x_{j_2}^{p_2} \wedge \cdots \wedge x_{j_l}^{p_l})$, with each *literal* $x_{j_i}^{p_i}$ is either a propositional variable $x_{j_i}^1 = x$ or its negation $x_{j_i}^0 = \bar{x}$. All remaining other lines are passed through unaltered. *Multiple controlled Toffoli gates (MCT)* are a subset from MPMCT gates in which the product terms can only consist of positive literals. The *NOT, CNOT, Toffoli (NCT)* library further restricts gates to have at most two control lines.

Example 1: Fig. 1a shows a Toffoli gate with mixed polarity control lines, the control lines are either denoted by $\bullet$ to indicate positive controls, or $\circ$ to indicate negated controls. The target line is denoted by $\bigoplus$. Fig. 1b shows different Toffoli gates in a cascade forming a reversible circuit. The annotated values demonstrate the computation of the gate for a given input assignment.

B. Quantum Circuits

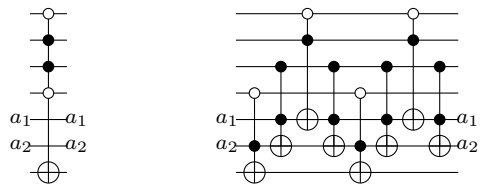
Instead of bits, quantum circuits manipulate qubits which can represent any complex combination of the classical Boolean values. In particular, a *qubit* $|\varphi\rangle$ is a vector $\binom{a}{b}$ where $a, b \in \mathbb{C}$ such that $|a|^2 + |b|^2 = 1$. We typically denote by $|0\rangle = \binom{1}{0}$ and $|1\rangle = \binom{0}{1}$ the *computational* basis vectors of $\mathbb{C}^2$, and associate them with the classical values 0 and 1, respectively.

Definition 3 (Quantum gate): In general, a quantum gate acting on n qubits/lines is represented by a $2^n \times 2^n$ unitary (norm-preserving) matrix [5]. As in reversible circuits, input lines may be designated as *control* lines, which have the effect of applying the gate whenever (possibly in superposition) the controlled qubit is in the $|1\rangle$ state.

The NCV and Clifford+T gate libraries contain quantum gates that realize the unitary matrices {NOT, CNOT, V, $V^\dagger$} and {NOT, CNOT, H, Z, S, $S^\dagger$, T, $T^\dagger$}, respectively. Both libraries are universal for reversible computation, though the Clifford+T library is more commonly used in fault tolerant quantum computing as it has known, simple implementations in most schemes. Details about the precise operations of the gates are not relevant for the scope of this paper.

Definition 4 (NCV-cost): The *NCV-cost* is the total number of NCV gates used in a quantum circuit.

Definition 5 (T-depth): The *T-depth* is the minimum number of T-stages in a quantum circuit where each stage consists of one or more T or $T^\dagger$ gates performed concurrently on separate qubits.



(a) 4-controlled gate (b) Barenco et al. (Lemma 7.2)

Fig. 2: Mapping an MPMCT gate into Toffoli gates using $(c-2)$ ancillas

Example 2: Figs. 1c and 1d present an optimal realization of a Toffoli gate with two positive controls based on the NCV library [4, Lemma 6.1] and Clifford+T library [10, Fig. 13], respectively. A Toffoli gate has an NCV-cost of 5 and a T-depth of 3 as it is outlined with the dashed rectangles.

C. Mapping Reversible Circuits to Quantum Circuits

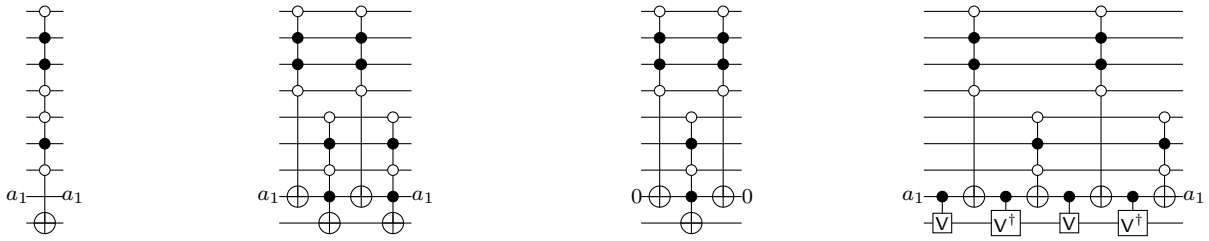
In order to derive a quantum circuit for a reversible function, the following approach is typically applied: (i) use synthesis to obtain a reversible circuit description, e.g., based on MPMCT gates; (ii) transform the circuit into one that consists only of NCT gates; (iii) map each Toffoli gate (with 2 controls) locally to a quantum circuit (all other gates in the NCT library are already quantum gates in the standard libraries). State-of-the art mapping approaches for the second step are inspired by the following two approaches presented in [4], mapping MCT gates into NCT circuits with linear complexity.

Barenco et al. (Lemma 7.2): According to [4, Lemma 7.2], when the number of available ancillas is $(c-2)$, a c-control MCT can be mapped directly to a circuit that consists of $4(c-2)$ Toffoli gates. The circuit depicted in Fig. 2b presents the circuit for the 4-control gate with 2 ancillas (see Fig. 2a). Maslov *et al.* [7] further optimized this algorithm to improve the NCV-cost by replacing each Toffoli with the more efficient Peres gate (NCV-cost of 4 versus 5 for a Toffoli). The T-depth remains the same in either case.

Barenco et al. (Lemma 7.3): According to [4, Lemma 7.3] a Toffoli gate $\mathrm{T}(C, t)$ with $|C| \geq 3$ is mapped to a cascade

$$\mathrm{T}(C_1, a_1) \circ \mathrm{T}(C_2 \cup \{a_1\}, t) \circ \mathrm{T}(C_1, a_1) \circ \mathrm{T}(C_2 \cup \{a_1\}, t) \quad (1)$$

where $C = C_1 \cup C_2$ and $C_1 \cap C_2 = \emptyset$. The ancilla a_1 can neither be in C, nor can it be t. If no free line is available, an additional line a_1 must be added to the circuit. Note that the cascade restores the value on a_1 and therefore it can be reused for all gates. Fig. 3b shows the resulting



(a) 7-controlled gate (b) Barenco et al. (Lemma 7.3) (c) Nielsen and Chuang (d) Miller et al.

Fig. 3: Mapping an MPMCT gate into smaller MPMCT gates using one ancilla

cascade after mapping a 7-controls MPMCT gate (see Fig. 3a). Note that after applying this algorithm, there exist a sufficient amount of ancilla lines for each gate to apply Lemma 7.2. Hence, the final circuit contains $8(c-3)$ Toffoli gates. Nielsen and Chuang [5], show that if the ancilla in the previous transformation is assigned to the 0 state, the fourth gate in (1) can be omitted (see Fig. 3c)—however, the ancilla can not be reused. The resulting circuit has $6(c-3)$ Toffoli gates.

Finally, Miller *et al.* [6] present an improved mapping based on Lemma 7.3 directly into quantum circuits by using the controlled-V gate (see Fig. 3d). In this case, the control set C_2 has one fewer line, at the expense of 4 controlled $V/V^\dagger$ gates. The resulting circuit contains $8(c-4)$ Toffoli gates and 4 NCV gates, reducing the total NCV-cost from $5 \cdot 4(c-2)$ to $4 \cdot 4(c-2)$.

In the rest of the paper, we denote the one ancilla optimized mapping algorithms of Barenco et al. given by Nielsen and Chuang, and Miller et al. by B1, NC, and MI, respectively. Also, we refer to the $(c-2)$ ancilla mapping algorithm from Barenco et al. as B2.

III. Clifford+T Aware Reversible Circuit Mapping

No effort has been spent on optimizing mapping approaches to Clifford+T quantum circuits. So far Clifford+T circuits have only been considered in pre- and post-mapping optimizations (see, e.g., [10]–[12]). In [13], the author has given a class of circuits whose T-depth can be reduced to one by using a sufficient number of ancillas.

In this paper, we propose mapping schemes that for the first time take into account the Clifford+T quantum gate library and the T-depth cost metric to enable more efficient fault-tolerant circuits. For a given reversible circuit on n lines consisting of gates $g_i = \mathrm{T}(C_i, t_i)$ the algorithm maps each gate according to the following case distinction, using $c = |C_i|$ to refer to the number of controls and $a = n - c - 1$ to refer to the number of free lines.

Case 1: ($c < 2$) The gate g_i is already contained in the Clifford+T gate library and is directly added to the quantum circuit.

Case 2: ($c = 2$) The gate g_i is mapped to its (T-depth) optimal quantum circuit according to Fig. 1d.

Case 3: ($a \geq \lceil \frac{c+1}{2} \rceil$) We apply a mapping scheme based on the B2 mapping that returns quantum circuits with a T-depth of $4(c-1)$ (see Section III-A).

Case 4: (*otherwise*) We map the gate with respect to a mapping scheme based on the B1, NC, or MI mapping (see Section III-B).

If there exists a gate $\mathrm{T}(C_i, t_i)$ such that $|C_i| = n-1$, we add one additional line to the circuit before starting the mapping. Thus, it is ensured that there exists at least one ancilla line when applying the mapping in Case 4.

A. Mapping using $(c-2)$ Ancillas

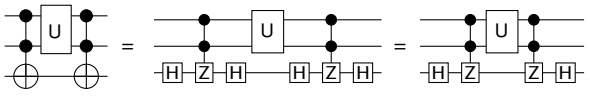
This section describes a mapping scheme based on the B2 mapping, using $c-2$ ancillas. We present the mapping by applying series of rewrites to the B2 mapping.

Lemma 1: A c-control MPMCT gate with $c \geq 4$ can be realized with a T-depth of

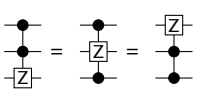
$$4(c-1) \tag{2}$$

using the B2 mapping with $c-2$ ancillas.

Consider a c-control MPMCT gate mapped using the B2 algorithm as shown in Fig. 2b. The standard mapping, using a T-depth 3 circuit for each Toffoli, results in a total T-depth of $3 \cdot 4(c-2) = 12(c-2)$. We may however rewrite the Toffoli gates with more efficient gates by noting that each Toffoli shares two lines with another Toffoli, and no gates occur in between. In particular, we first rewrite every Toffoli with a doubly-controlled Z gate and two Hadamard gates on either side of the target line. For matched pairs of Toffoli gates sharing a target, the Hadamard gates cancel:



Recall that controlled phase gates are symmetric in that the target behaves like a control [14], i.e.,



By applying this fact (see Fig. 4a), we may observe that each doubly-controlled Z gate now shares exactly two controls with another gate. We may now use the iZ-gate construction of Selinger [13] to rewrite each doubly-controlled Z gate using fewer T gates. Explicitly, we define the iZ-gate as the operator

$$iZ : |xyz\rangle \mapsto \omega^{4xyz-2xy}|xyz\rangle \tag{3}$$

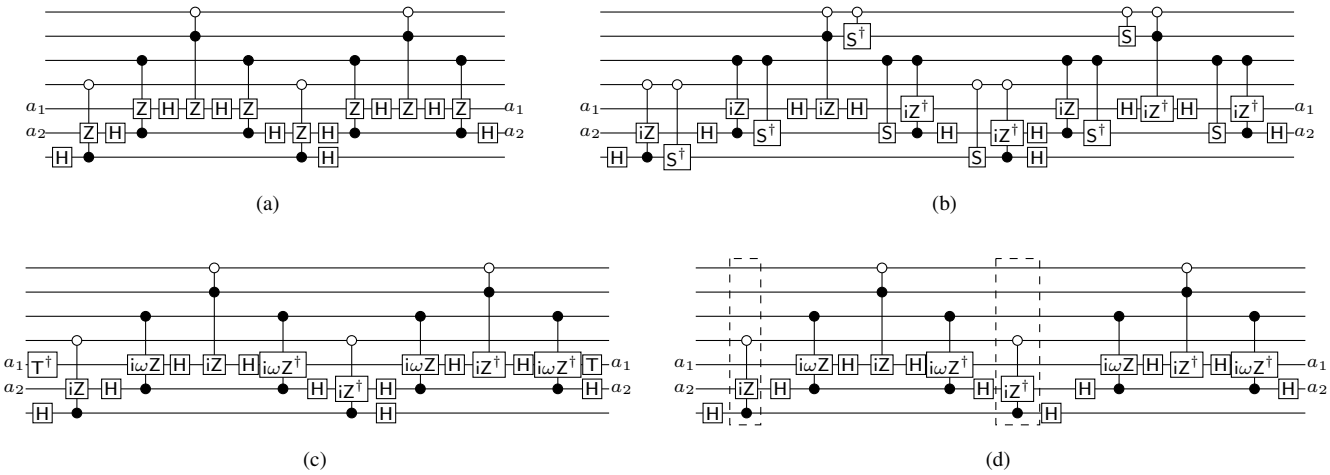
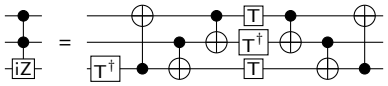


Fig. 4: Optimization of Barenco et al. algorithm (Lemma 7.2) wrt. T-depth

where $\omega = e^{\frac{i\pi}{4}}$. We also denote the inverse of the iZ gate by $iZ^\dagger$. The iZ gate implements the doubly-controlled Z gate up to some smaller phase using only 4 T-gates:



For each pair of doubly-controlled Z gates that share two controls, one is written as an iZ gate and a singly-controlled $S^\dagger$ gate, and the other is written as an $iZ^\dagger$ and a singly-controlled S gate (see Fig. 4b) – the controlled $S/S^\dagger$ gates then cancel.

To further optimize this mapping, we give a refinement of the iZ gate – the $i\omega Z$ gate

$$i\omega Z : |xyz\rangle \mapsto \omega^{4xyz-2xy-z}|xyz\rangle \tag{4}$$

where $\omega = e^{\frac{i\pi}{4}}$ and $i\omega Z^\dagger$ is its inverse. This gate may be implemented in T-depth 1, and together with a $T^\dagger$ gate on the target implements the iZ gate:

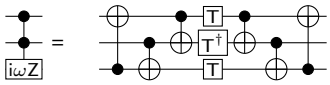
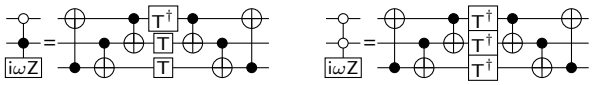


Fig. 4b shows the B2 mapping of the 5 control MCT gate where iZ gates have been replaced with $i\omega Z/i\omega Z^\dagger$ gates, and the T gates are either cancelled or parallelized (see Fig. 4c). Note that the 4 "points" of the cascade are left as iZ gates since they cannot be parallelized further. The extra phase gates from the outermost cascades (see Fig. 4c) are also cancelled despite being physically separated in the circuit, since each ancilla is returned to its initial state as shown in Fig. 4d.

To complete the analysis, we note that each $iZ/iZ^\dagger$ gate can be mapped to 4 T gates in depth 2 [13], while each $i\omega Z/i\omega Z^\dagger$ gate can be mapped into a quantum circuit with a T-depth of 1. Similarly for mixed polarity gates:



This gives a total T-depth of $4(c-2)+4 = 4(c-1)$.

Note that this bound beats out the T-depths achieved by the state-of-the-art approach Tpar [10], showing that their heuristic approach is non-optimal in some cases.

B. Mapping using One Ancilla

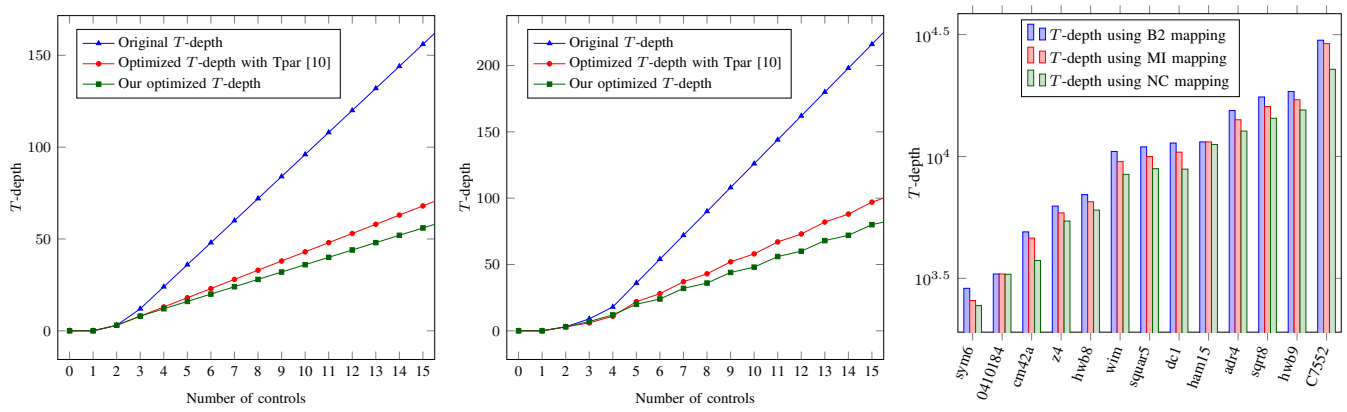
In this section we give optimized mapping schemes using one ancilla based on the B1, NC and MI mappings. In each case, a c-control MPMCT gate is decomposed into m-control and $(c-m+1)$-control (or $(c-m)$-control if the case of the MI mapping) MPMCT gates, which are further decomposed using the optimized B2 mapping explained above.

Lemma 2: A c-control MPMCT gate with $c \geq 5$ controls can be realized with a T-depth of

$$8(c-2) \quad \text{based on the B1 mapping,} \tag{5}$$
$$6(c-2)+2 \quad \text{based on the NC mapping, and} \tag{6}$$
$$8(c-3)+4 \quad \text{based on the MI mapping} \tag{7}$$

Consider the B1 mapping as in Fig. 3b. In this case the standard mapping (using a T-depth 3 Toffoli) gives a total T-depth of $24(c-3)$. However if we map the first two MPMCT gates using the B2 mapping above, then use the *inverse* (obtained by reversing the circuit and replacing each T gate with $T^\dagger$) of the B2 mapping for the remaining MPMCT gates, we can cancel an additional 8 T gates. Specifically, for each pair of MPMCT gates (first and third or second and fourth), the value on the target line of either dashed iZ gate shown in Fig. 4d is constant. As in the proof of the B2 upper bounds, we may then replace each dashed iZ gate with an $i\omega Z$ gate and cancel the extra T gates. The result is a total reduction of 8 levels of T-depth, giving a total T-depth for a c-control MPMCT gate of $2{\cdot}4(m-1)+2{\cdot}4(c+1-m-1)-8 = 8(c-2)$.

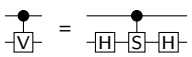
For the NC mapping we may use the same argument to cancel an additional 2 T-gates each from the first and third MPMCT gates. The resulting mapping has a T-depth of $6(c-2)$ when c is even and $6(c-2)+2$ when c is odd, compared to a T-depth of $18(c-3)$ when using the standard mapping.



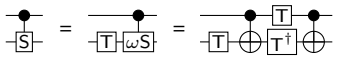
(a) MPMCT mapping using B1 (b) MPMCT mapping using NC (c) Circuits Mapping

Fig. 5: T-depth for MPMCT gates and reversible circuits

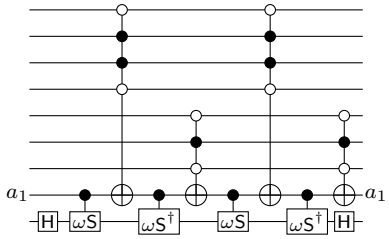
Finally, consider the MI mapping. The T-depth under the standard mapping in this case is $24(c-4)+8$. We arrive at our T-depth $8(c-3)+4$ by using the same argument to reduce each of the 4 multiple control Toffoli gates by two layers of T-depth. We further note that each controlled V gate may be mapped in T-depth 1. In particular, we first map each controlled V to controlled S gates conjugated by Hadamards:



As in the B2 mapping, adjacent Hadamards cancel, then the controlled S gates are alternately mapping into ωS and $\omega S^\dagger$ gates with the following mapping:



where $\omega S : |xy\rangle \mapsto \omega^{2xy-y}|xy\rangle$. The additional $T/T^\dagger$ gates cancel, leaving 4 $\omega S/\omega S^\dagger$ gates as follows:



Each such gate is finally mapped to two $T/T^\dagger$ gates in T-depth 1, giving a total T-depth for the MI mapping scheme of $2\cdot 4(m-1)+2\cdot 4(c-m-1)-8+4=8(c-3)+4$.

While the NC mapping clearly gives the best T-depth, it should be noted that it does so by using a zero-valued ancilla and so may require an extra line to be added where the B1 and MI mappings do not.

IV. Experimental Results

In this section we provide the experimental results of our proposed approaches for mapping MPMCT gates into quantum circuits with gates from the Clifford+T gate library. The mapping approaches above have been implemented in the open source toolkit *RevKit* [15] and tested on a suite of benchmarks taken from [16], [17]. The reversible functions were synthesized with the approach outlined in [3].

A. Mapping of MPMCT Gates

The experimental results presented graphically in the plot in Fig. 5a show the T-depth of mapped MPMCT gates with up to 15 controls based on B2. The values of the x-axis and the y-axis denote the number of controls and the *T-depth*, respectively. The plot contains three different scenarios: the *T-depth* of the of MPMCT gates mapped using the original B2 (in blue), the *T-depth* of the mapped MPMCT using B2 and then optimized with Tpar [10] (in red), and the *T-depth* of the of MPMCT gates mapped using the optimized B2 (in green) as described in Section III-A. We achieved the smallest T-depth for each MPMCT gate in comparison with the two others. The overall improvement of the T-depth reaches 60% with respect to the original B2, while 14% with respect to Tpar.

For the mapping based on one ancilla, we only report the best mapping, i.e., the NC algorithm. The plots in Fig. 5b shows the T-depth of mapped MPMCT for up to 15 controls using NC. It is clear that the results of the enhanced mapping approach are significantly better than the original NC mapping approaches as well as the optimized realizations with Tpar.

B. Mapping of Reversible Circuits

First, we compared the efficiency of each mapping algorithm with respect to the obtained T-depth. The plot in Fig. 5c shows the T-depth of each circuit using the three different mapping strategies B1 (blue), NC (green), and MI (red). As it is expected, since the MI approach is an improvement of the B1 algorithm, we clearly see that MI outperforms B1. While NC beats each of the previous mentioned algorithms, this is explained by the fact of omitting an MPMCT gate on the mapping due to the use of an ancilla line set to the constant value 0. An interesting question for future research is when the cost of adding extra 0-valued ancillas outweighs the extra T-depth incurred by using the B1 or MI approach.

TABLE I: Experimental Results

Benchmark			Nielsen Chuang [5] Mapping			
ID	L	G	T_0	T_1	Time	I_{TD}
4_49_7	4	14	84	60	0.00	28.57%
4gt10	5	19	233	145	0.00	37.77%
decod24-en.	6	30	472	292	0.00	38.14%
majority	6	70	1154	726	0.00	37.09%
f2	7	96	2811	1591	0.00	43.40%
sym6	7	163	4590	2566	0.01	44.10%
z4	8	329	11756	5868	0.02	50.09%
hwb8	8	372	13000	6520	0.02	49.85%
wim	9	364	20583	9527	0.04	53.71%
squar5	9	394	21593	9985	0.04	53.76%
adr4	9	606	30182	14146	0.04	53.13%
sqrt8	9	666	34175	16027	0.05	53.10%
hwb9	9	807	36105	17089	0.05	52.67%
dc1	10	273	24596	10416	0.04	57.65%
5xp1	10	1046	69920	29592	0.12	57.68%
root	10	1135	75087	31639	0.13	57.86%
dist	10	1283	85515	35915	0.14	58.00%
max46	10	1449	90958	38210	0.12	57.99%
urf3	10	1486	94924	39876	0.12	57.99%
life	10	1577	100216	42332	0.12	57.76%
9symml	10	1578	88227	36897	0.11	58.18%
sym9	10	1610	95896	40272	0.15	58.00%
rd84	11	2901	214922	92146	0.37	57.13%
clip	11	3138	224223	96555	0.41	56.94%
sym10	11	3539	263606	113062	0.44	57.11%
cm152a	11	3804	267836	115216	0.33	56.98%
urf4	11	3831	272048	116988	0.34	57.00%
plus63-4096	12	18	838	346	0.00	58.71%
cycle10	12	27	1606	690	0.00	57.04%
sqr6	12	2365	287561	114281	0.45	60.26%
plus127-192	13	19	1018	422	0.00	58.55%
plus63-8192	13	20	1066	442	0.01	58.54%
cm42a	13	73	11952	4628	0.02	61.28%
dc2	13	5696	807824	320580	1.33	60.32%
0410184	14	193	7707	3295	0.01	57.25%
misex1	14	5242	931174	357574	1.43	61.60%
ham15	15	1114	21555	11203	0.03	48.03%
urf6	15	2350	540128	201976	0.62	62.61%
C7552	20	274	80456	29040	0.12	63.91%
bw	32	3709	2205808	769364	3.02	65.12%
Average						**54.75%**

Due to lack of space, we report the numerical experiments of the most interesting mapping (optimized NC together with optimized B2). Obtained results are shown in Table I. For each benchmark we show the name (ID), the number of lines (L), and the number of gates (G). Then we apply the mapping algorithm NC when the gate has no sufficient ancillas to apply B2. We give the T-depth of the original mapping algorithm (T_0), the T-depth of the improved mapping algorithm (T_1), the needed run-time (Time), and the T-depth improvement I_{TD}, respectively. Experiments demonstrate the efficiency of the proposed mapping methodologies wrt. original mapping algorithms. Compared to the best previously introduced methods, we show that our mapping yields substantially smaller circuits. More precisely, improvements of around 54% can be achieved on average for the optimized NC algorithm. In the best case, the T-depth of the circuits can even be reduced by more than 65% (*bw*).

V. Summary and Conclusions

In this work, we extended and improved the existing mapping algorithms of reversible circuits into quantum circuits using the Clifford+T quantum library. No such mapping algorithm has been presented for the Clifford+T gate library before. As shown, the new mapping approaches lead to circuits with lower T-depth compared to standard mappings, on average by more than 54% for the combined NC & B2 mapping strategy.

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